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DESCRIPTION

ENCODING METHOD, ENCODING APPARATUS, DECODING METHOD, DECODING APPARATUS AND PROGRAMS THEREOF

TECHNICAL FIELD

[0001] The present invention relates to an encoding method for encoding an orthogonal transformation coefficient, an encoding apparatus and a program thereof, a decoding method for decoding the same, a decoding apparatus and a program thereof.

BACKGROUND ART

[0002] In recent years, an apparatus based on the MPEG (Moving Picture Experts Group) and other methods for compressing by discrete cosine transformation or other orthogonal transformation and motion compensation, wherein image data is handled as digital and redundancy peculiar to image information is utilized for highly efficient transmission and accumulation of information, has become widespread both in distributing information by broadcasting stations, etc. and receiving information in general households.

[0003] The MPEG2 and MPEG4 methods are followed by a proposal for an encoding method called an MPEG4/AVC (Advanced Video Coding).

In an encoding apparatus of the MPEG4/AVC method, orthogonal transformation is performed on image data to be encoded in units of block data having a size of, for example, 4×4; and non-0 coefficients quantity data indicating a quantity of non-0 transformation coefficients included in transformation coefficients of the block data obtained thereby is subjected to variable length coding based on a plurality of correspondence data (VLC table), each regulating correspondence of a value of non-0 coefficient quantity data by the number of 4^2 to an encoding code thereof.

Here, the plurality of correspondence data regulates, so that bit lengths of the non-0 coefficient quantity data indicating "0" are different from one another and the maximum bit length of an encoding code used in the correspondence data becomes longer, as a bit length of non-0 coefficient quantity data indicating "0" becomes shorter.

Also, in the above encoding apparatus, the encoding efficiency is improved by selecting correspondence data; wherein an encoding code having a longer bit length is assigned to the non-0 coefficient quantity data indicating "0", as the number of variable coefficients excepting "0" and "1" becomes increased in transformation coefficients of block data around the 4×4 block data to

be encoded.

DISCLOSURE OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0004] In the encoding apparatus described above, however, orthogonal transformation is sometimes performed in units of block data having a block size of 8×8 (8×8 block data).

However, the correspondence data of the related art described above corresponds only to a value of non-0 coefficient quantity data by the number of 4^2, and an encoding code of non-0 coefficient quantity data by the number of 8^2 obtained by performing orthogonal transformation on 8×8 block data cannot be obtained.

[0005] The present invention has been made in consideration of the above circumstances and provides an encoding method, an encoding apparatus and the program for performing encoding on non-0 coefficient quantity data of transformation coefficients obtained by orthogonal transformation of image block data having a second block size, which is a multiple of a first block size, based on correspondence data conforming to the first block size.

MEANS FOR SOLVING THE PROGRAM

[0006] To overcome the above disadvantages of the related art described above and to achieve the above

object, according to a first aspect of the present invention, there is provided an encoding method for performing variable length encoding by using correspondence data on non-0 coefficient quantity data indicating a quantity of non-0 transformation coefficients in a plurality of transformation coefficients obtained by performing orthogonal transformation on image block data including: when, for respective possible values of the non-0 coefficient quantity data in the image block data having a first block size, using a plurality of correspondence data each regulating correspondence of the non-0 coefficient quantity data to the encoding code, so that bit lengths of non-0 coefficient quantity data indicating "0" become different from one another, and the maximum bit length of the encoding codes to be used by the correspondence data becomes longer as the bit lengths of the non-0 coefficient quantity data indicating "0" becomes shorter; a first step for assigning a plurality of transformation coefficients obtained by performing orthogonal transformation on image block data having a second block size, which is a multiple of the first block size, to one sub block data in accordance with a frequency corresponding to the transformation coefficients among a plurality of sub block data composed of the

transformation coefficients by the same number as that in image block data having the first block size; a second step for generating the non-0 coefficient quantity data for each of the plurality of sub block data based on the transformation coefficients assigned to the sub block data in the first step; and a third step for determining the encoding codes to be assigned to the non-0 coefficient quantity data generated in the second step for each of the plurality of sub block data by using the correspondence data in which an encoding code having a shorter bit length is assigned to the non-0 coefficient quantity data indicating "0" comparing with the correspondence data used for other sub block data on the direct current component side with respect to the sub block data.

[0007] According to a second aspect of the present invention, there is provided an encoding apparatus for performing variable length encoding by using correspondence data on non-0 coefficient quantity data indicating a quantity of non-0 transformation coefficients in a plurality of transformation coefficients obtained by performing orthogonal transformation on image block data, including: when, for respective possible values of the non-0 coefficient quantity data in the image block data having a first

block size, using a plurality of correspondence data each regulating correspondence of the non-0 coefficient quantity data to the encoding code, so that bit lengths of non-0 coefficient quantity data indicating "0" become different from one another, and the maximum bit length of the encoding codes to be used by the correspondence data becomes longer as the bit lengths of the non-0 coefficient quantity data indicating "0" becomes shorter; an assigning means for assigning a plurality of transformation coefficients obtained by performing orthogonal transformation on image block data having a second block size, which is a multiple of the first block size, to one sub block data in accordance with a frequency corresponding to the transformation coefficients among a plurality of sub block data composed of the transformation coefficients by the same number as that in image block data having the first block size; a generating means for generating the non-0 coefficient quantity data for each of the plurality of sub block data based on the transformation coefficients assigned to the sub block data by the assigning means; and an encoding means for determining the encoding codes to be assigned to the non-0 coefficient quantity data generated by the generation means for each of the plurality of sub block data by using the correspondence data in which an

encoding code having a shorter bit length is assigned to the non-0 coefficient quantity data indicating "0" comparing with the correspondence data used for other sub block data on the direct current component side with respect to the sub block data.

[0008] An operation of the second aspect of the present invention is as below.

The assigning means assigns a plurality of transformation coefficients obtained by performing orthogonal transformation on image block data having a second block size, which is a multiple of a first block size, to one sub block data in accordance with a frequency corresponding to the transformation coefficients among a plurality of sub block data composed by the same number of the transformation coefficients as the number of image block data having the first block size.

Next, the generating means generates the non-0 coefficient quantity data for each of the plurality of sub block data based on the transformation coefficients assigned to the sub block data by the assigning means.

Next, the encoding means determines the encoding code to be assigned to the non-0 coefficient quantity data generated by the generating means for each of the plurality of sub block data by using the correspondence

data in which an encoding code having a shorter bit length is assigned to the non-0 coefficient quantity data indicating "0" comparing with the correspondence data used for other sub block data on the direct current component side with respect to the sub block data.

[0009] According to a third aspect of the present invention, there is provided a program to be executed by a computer to perform encoding processing of variable length encoding by using correspondence data on non-0 coefficient quantity data indicating a quantity of non-0 transformation coefficients in a plurality of transformation coefficients obtained by performing orthogonal transformation on image block data, by which: when, for respective possible values of the non-0 coefficient quantity data in the image block data having a first block size, using a plurality of correspondence data each regulating correspondence of the non-0 coefficient quantity data to the encoding code, so that bit lengths of non-0 coefficient quantity data indicating "0" become different from one another, and the maximum bit length of the encoding codes to be used by the correspondence data becomes longer as the bit lengths of the non-0 coefficient quantity data indicating "0" becomes shorter; a first procedure for assigning a plurality of transformation coefficients obtained by

performing orthogonal transformation on image block data having a second block size, which is a multiple of the first block size, to one sub block data in accordance with a frequency corresponding to the transformation coefficients among a plurality of sub block data composed of the transformation coefficients by the same number as that in image block data having the first block size; a second procedure for generating the non-0 coefficient quantity data for each of the plurality of sub block data based on the transformation coefficients assigned to the sub block data in the first procedure; and a third procedure for determining the encoding codes to be assigned to the non-0 coefficient quantity data generated in the second procedure for each of the plurality of sub block data by using the correspondence data in which an encoding code having a shorter bit length is assigned to the non-0 coefficient quantity data indicating "0" comparing with the correspondence data used for other sub block data on the direct current component side with respect to the sub block data; are executed by the computer.

[0010] According to a fourth aspect of the present invention, there is provided a decoding method, for assigning transformation coefficients obtained by performing orthogonal transformation on image data to be

encoded in units of block data having a second block size, which is a multiple of a first block size, to a plurality of sub block data in accordance with frequencies related to the transformation coefficients; generating non-0 coefficient quantity data indicating a quantity of non-0 transformation coefficients in transformation coefficients composing the sub block data for each of the plurality of sub block data; and, when an encoding code of the non-0 coefficient quantity data is obtained by using predetermined correspondence data, retrieving the non-0 coefficient quantity data from the encoding code by using the correspondence data, including: when, for respective possible values of the non-0 coefficient quantity data in the image block data having a first block size, using a plurality of correspondence data each regulating correspondence of the non-0 coefficient quantity data to the encoding code, so that bit lengths of non-0 coefficient quantity data indicating "0" become different from one another, and the maximum bit length of the encoding codes to be used by the correspondence data becomes longer as the bit lengths of the non-0 coefficient quantity data indicating "0" becomes shorter; a first step for determining the non-0 coefficient quantity data of each of the encoding codes of the plurality of sub block data by using the correspondence

data, wherein an encoding code having a longer bit length comparing with that in the correspondence data used for the sub block data on the direct current component side and the non-0 coefficient quantity data indicating "0" are related for the sub block data; a second step for generating the transformation coefficients composing the sub block data based on the non-0 coefficient quantity data determined in the first step for each of the plurality of sub block data; and a third step for relocating the transformation coefficients generated in the second step and obtaining transformation coefficients of the block data having the second block size.

[0011] According to a fifth aspect of the present invention, there is provided a decoding apparatus, for assigning transformation coefficients obtained by performing orthogonal transformation on image data to be encoded in units of block data having a second block size, which is a multiple of a first block size, to a plurality of sub block data in accordance with frequencies corresponding to the transformation coefficients; generating non-0 coefficient quantity data indicating a quantity of non-0 transformation coefficients in transformation coefficients composing the sub block data for each of the plurality of sub block data; and, when an encoding code of the non-0 coefficient quantity data is

obtained by using predetermined correspondence data, retrieving the non-0 coefficient quantity data from the encoding code by using the correspondence data, including: when, for respective possible values of the non-0 coefficient quantity data in the image block data having the first block size, using a plurality of correspondence data each regulating correspondence of the non-0 coefficient quantity data to the encoding code, so that bit lengths of non-0 coefficient quantity data indicating "0" become different from one another, and the maximum bit length of the encoding codes to be used by the correspondence data becomes longer as the bit lengths of the non-0 coefficient quantity data indicating "0" becomes shorter; a determining means for determining the non-0 coefficient quantity data of each of the encoding codes of the plurality of sub block data by using the correspondence data, wherein an encoding code having a longer bit length comparing with that in the correspondence data used for the sub block data on the direct current component side and the non-0 coefficient quantity data indicating "0" are related for the sub block data as the bit lengths of non-0 coefficients quantity data indicating "0" becomes shorter; a generating means for generating the transformation coefficients composing the sub block data based on the

non-0 coefficient quantity data determined in the determining means for each of the plurality of sub block data; and a retrieving means for relocating the transformation coefficients generated by the generating means and obtaining transformation coefficients of the block data having the second block size.

[0012] An operation of the fifth aspect of the present invention is as below.

The determining means determines the non-0 coefficient quantity data of each of the encoding codes of a plurality of sub block data by using the correspondence data, wherein the non-0 coefficient quantity data indicating "0" and an encoding code having a longer bit length comparing with that in the correspondence data used for the sub block data on the direct current components side are related for the sub block data.

Next, the generating means generates the transformation coefficients composing the sub block data for each of the plurality of sub block data based on the non-0 coefficient quantity data determined by the determining means.

Next, the retrieving means relocates the transformation coefficients generated by the generating means and obtains transformation coefficient of the block

data having the second block size.

[0013] According to a sixth aspect of the present invention, there is provided a program to be executed by a computer, for assigning transformation coefficients obtained by performing orthogonal transformation on image data to be encoded in units of block data having a second block size, which is a multiple of a first block size, to a plurality of sub block data in accordance with frequencies related to the transformation coefficients; generating non-0 coefficient quantity data indicating a quantity of non-0 transformation coefficients in transformation coefficients composing the sub block data for each of the plurality of sub block data; and, when an encoding code of the non-0 coefficient quantity data is obtained by using predetermined correspondence data, retrieving the non-0 coefficient quantity data from the encoding code by using the correspondence data, by which: when, for respective possible values of the non-0 coefficient quantity data in the image block data having the first block size, using a plurality of correspondence data each regulating correspondence of the non-0 coefficient quantity data to the encoding code, so that bit lengths of non-0 coefficient quantity data indicating "0" become different from one another, and the maximum bit length of the encoding codes to be used by the

correspondence data becomes longer as the bit lengths of the non-0 coefficient quantity data indicating "0" becomes shorter; a first procedure for determining the non-0 coefficient quantity data of each of the encoding codes of the plurality of sub block data by using the correspondence data, wherein an encoding code having a longer bit length comparing with that in the correspondence data used for the sub block data on the direct current component side and the non-0 coefficient quantity data indicating "0" are related for the sub block data; a second procedure for generating the transformation coefficients composing the sub block data based on the non-0 coefficient quantity data determined in the first procedure for each of the plurality of sub block data; and a third procedure for relocating the transformation coefficients generated in the second procedure and obtaining transformation coefficients of the block data having the second block size; are executed by the computer.

EFFECT OF THE INVENTION

[0014] According to the present invention, it is possible to provide an encoding method, an encoding apparatus and the program for encoding non-0 coefficient quantity data of transformation coefficients obtained by performing orthogonal transformation on image block data

having a second block size being a multiple of a first block size, based on correspondence data conforming to the first block size.

Also, according to the present invention, a decoding method, a decoding apparatus and the program for decoding an encoding code obtained by the above encoding can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] [FIG. 1] FIG. 1 is a view of a configuration of a communication system of a first embodiment according to the present invention.

[FIG. 2] FIG. 2 is a functional block diagram of an encoding apparatus shown in FIG. 1.

[FIG. 3] FIG. 3 is a view of a configuration of a reversible coding circuit shown in FIG. 2.

[FIG. 4] FIGs. 4A and 4B are views for illustrating an order that a scanning circuit shown in FIG. 3 scans orthogonal transformation of 4×4 block data.

[FIG. 5] FIG. 5 is a view for illustrating an order that a scanning circuit shown in FIG. 3 scans orthogonal transformation of 8×8 block data.

[FIG. 6] FIG. 6 is a view for illustrating a method that a run level calculation circuit generates non-0 coefficient quantity data "TotalCoeff" of 4×4 block data and final continuing quantity data "TrailingOne".

[FIG. 7] FIGs. 7A and 7B are views for illustrating a method that a two-dimensional reversible encoding circuit shown in FIG. 3 performs encoding on non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOne" of 4×4 block data.

[FIG. 8] FIG. 8 is a view for illustrating a method that the two-dimensional reversible encoding circuit shown in FIG. 3 performs encoding on non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOne" of 8×8 block data.

[FIG. 9] FIG. 9 is a view for illustrating a method that a two-dimensional reversible encoding circuit shown in FIG. 3 performs encoding on non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOne" of 8×8 block data.

[FIG. 10] FIG. 10 is a view for illustrating an operation example of the reversible encoding circuit shown in FIG. 3.

[FIG. 11] FIG. 11 is a view of a configuration of a decoding apparatus shown in FIG. 1.

[FIG. 12] FIG. 12 is a view of a configuration of a reversible decoding circuit shown in FIG. 11.

LIST OF REFERENCES

[0016] 1...communication system, 2...encoding apparatus, 3...decoding apparatus, 22...A/D conversion

circuit, 23...screen relocating circuit, 24...computing circuit, 25...orthogonal transformation circuit, 26...quantization circuit, 27...reversible encoding circuit, 28...buffer memory, 29...inverse quantization circuit, 30...inverse orthogonal transformation circuit, 31...frame memory, 32...rate control circuit, 33...adding circuit, 41...intra-prediction circuit, 42...motion prediction compensation circuit, 45...orthogonal transformation size determination circuit, 51...scanning circuit, 52...sub block generation circuit, 53...run level calculation circuit, 54...two-dimensional reversible encoding circuit, 55...revel encoding circuit, 56...run encoding circuit, 57...multiplexing circuit, 81...buffer memory, 82...reversible decoding circuit, 83...inverse quantization circuit, 84...inverse orthogonal transformation circuit, 85...addition circuit, 86...frame memory, 87...screen relocating buffer, 88...D/A conversion circuit, 110...separation circuit, 111...two-dimensional reversible decoding circuit, 112...level decoding circuit, 113...run decoding circuit, 114...transformation coefficient recovery circuit, 115...block recovery circuit, 116...scan transformation circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

[0017] Below, an encoding apparatus according to

embodiments of the present invention will be explained.

First, correspondence of components of the present embodiments and components of the present invention will be explained.

A 4×4 block size in the present embodiment corresponds to the first block size in the present invention, and an 8×8 block size in the present embodiment corresponds to the second block size in the present invention.

Also, a non-0 coefficient quantity data "TotalCoeff" in the present embodiment corresponds to the non-0 coefficient quantity data in the present invention.

Also, numbers on a right side in Table 1 correspond to encoding codes of the present invention.

Transformation table data TRNa1, 2, 3 and 4 shown in Table 1 correspond to correspondence data in the present invention.

Also, sub block data SB1, SB2, SB3 and SB4 shown in FIG. 8 correspond to sub block data in the present invention.

[0018] Steps ST17 and ST18 in FIG. 10 correspond to the first step of the first aspect of the present invention, a step ST19 corresponds to the second step, and steps ST21 and ST22 correspond to the third step.

Also, a step ST13 in FIG. 10 corresponds to the

fourth step of the first aspect of the present invention, steps ST14 and ST15 correspond to the fifth step, and a step ST16 corresponds to the sixth step.

A scanning transformation circuit 51 and sub block generation circuit 52 shown in FIG. 3 correspond to the assigning means of the second aspect of the present invention.

Also, a run level calculation circuit 53 shown in FIG. 3 corresponds to the generation means of the second aspect of the present invention, and a two-dimensional reversible encoding circuit 54 corresponds to the encoding means of the second aspect of the present invention.

[0019] A two-dimensional reversible decoding circuit 111 shown in FIG. 12 corresponds to the determining means of the fifth aspect of the present invention, a transformation coefficient recovery circuit 114 corresponds to the generating means of the fifth aspect of the present invention, and a block recovery circuit 115 corresponds to the retrieving means of the fifth aspect of the present invention.

[0020] Below, a communication system 1 in the present embodiment will be explained.

First, correspondence of components of the present embodiment and components of the present invention will

be explained.

FIG. 1 is a conceptual view of the communication system 1 of the present embodiment.

As shown in FIG. 1, the communication system 1 has an encoding apparatus 2 provided on the transmission side and a decoding apparatus 3 provided on the receiving side.

The encoding apparatus 2 corresponds to the data processing apparatus and the encoding apparatus of the present invention.

In the communication system 1, frame image data (a bit stream) compressed by orthogonal transformation, such as discrete cosine transformation and Karhunen-Loeve transformation, and motion compensation is generated, modulated, then, transmitted via transmission media, such as satellite broadcast wave, cable TV network, telephone line network and cellular-phone network, in the encoding apparatus 2 on the transmission side.

On the receiving side, after demodulating an image signal received in the decoding apparatus 3, frame image data expanded by inverse transformation of the orthogonal transformation and motion compensation by the above modulation is generated and used.

Note that the transmission media may be an optical disk, a magnetic disk, a semiconductor memory and other recording media.

[0021] [Encoding Apparatus 2]

Below, the encoding apparatus 2 in FIG. 1 will be explained.

FIG. 2 is a view of the overall configuration of the encoding apparatus 2 in FIG. 1.

As shown in FIG. 2, the encoding apparatus 2 includes, for example, an A/D transformation circuit 22, a screen relocating circuit 23, a computing circuit 24, an orthogonal transformation circuit 25, a quantization circuit 26, a reversible encoding circuit 27, a buffer memory 28, an inverse quantization circuit 29, an inverse orthogonal transformation circuit 30, a frame memory 31, a rate control circuit 32, an adding circuit 33, an intra-prediction circuit 41, a motion prediction compensation circuit 42 and an orthogonal transformation size determination circuit 45.

[0022] Below, components of the encoding apparatus 2 will be explained.

[A/D Conversion Circuit 2]

The A/D conversion circuit 22 converts an input original image signal S10 composed of an analog luminance signal Y and color-difference signals Pb and Pr to digital picture data S22 and outputs the same to the screen relocating circuit 23.

[0023] [Screen Relocating Circuit 23]

The screen relocating circuit 23 relocates frame data in the picture data S22 input from the A/D conversion circuit 22 to be in an encoding order in accordance with the GOP (group of pictures) structure formed by picture types I, P and B of the frame data so as to obtain original image data S23, and outputs the same to the computing circuit 24, the motion prediction compensation circuit 42 and the intra-prediction circuit 41.

[0024] [Computing Circuit 24]

The computing circuit 24 generates image data S24 indicating a difference between the original image data S23 and prediction image data input from the intra-prediction circuit 41 or the motion prediction compensation circuit 42 and outputs the same to the orthogonal transformation circuit 25.

[0025] [Orthogonal Transformation Circuit 25]

The orthogonal transformation circuit 25 performs orthogonal transformation, such as discrete cosine transformation (DCT) and Karhunen-Loeve transformation, on the image data S24 to generate image data (for example, a DCT coefficient) S25 indicating a transformation coefficient and outputs the same to the quantization circuit 26.

The orthogonal transformation circuit 25 performs

orthogonal transformation on the image data S24 input from the computing circuit 24 by an orthogonal transformation size specified by an orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 to generate the image data S25 indicating a transformation coefficient.

In the present embodiment, block sizes of 4×4 and 8×8 are used as the orthogonal transformation size.

[0026] [Quantization Circuit 26]

The quantization circuit 26 performs quantization on the image data S25 (transformation coefficient before quantization) based on the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 and a quantization scale QS input from the rate control circuit 32 so as to generate image data S26 indicating a transformation coefficient after quantization and outputs the same to the reversible encoding circuit 27 and the inverse quantization circuit 29.

For example, when the orthogonal transformation circuit 25 selects one of the 4×4 and 8×8 and performs orthogonal transformation to an accuracy of integers, a suitable coefficient to be used in normalization processing in the quantization circuit 26 is different

between the 4×4 and 8×8. Therefore, the quantization circuit 26 corrects the quantization scale QS input from the rate control circuit 32 based on the orthogonal transformation size indicated by the orthogonal transformation size signal TRSIZE, and quantizes the image data S25 by using the corrected quantization scale.

[0027] [Reversible Encoding Circuit 27]

The reversible encoding circuit 27 stores in the buffer memory 28 image data obtained by performing variable length encoding on the image data S26.

At this time, the reversible encoding circuit 27 stores in head data, etc. a motion vector MV input from the motion prediction compensation circuit 42 or a differential motion vector thereof, identification data of reference image data, and an intra-prediction mode input from the intra-prediction circuit 41.

The reversible encoding circuit 27 performs reversible encoding processing in accordance with respective orthogonal transformations of 4×4 block size and 8×8 block size.

The encoding processing by the reversible encoding circuit 27 will be explained in detail later on.

[0028] [Buffer Memory 28]

Image data stored in the buffer memory 28 is subjected to modulation, etc. and transmitted as image

data S2.

The image data S2 is decoded by the decoding apparatus 3, which will be described later on.

[Inverse Quantization Circuit 29]

The inverse quantization circuit 29 performs inverse quantization corresponding to quantization by the quantization circuit 26 on the image data S26, generates data obtained thereby, and outputs the same to the inverse orthogonal transformation circuit 30.

[Inverse Orthogonal Transformation Circuit 30]

The inverse orthogonal transformation circuit 30 performs inverse transformation of the orthogonal transformation by the orthogonal transformation circuit 25 on the data input from the inverse quantization circuit 29 to generate image data and outputs the same to the adding circuit 33.

[Adding Circuit 33]

The adding circuit 33 adds the (decoded) image data input from the inverse orthogonal transformation circuit 30 and prediction image data PI input from the selection circuit 44 to generate reference (restructured) picture data R_PIC and writes the same in the frame memory 31.

Note that a de-block filter may be provided between the adding circuit 33 and the frame memory 31. The de-block filter writes in the frame memory 31 image data

obtained by eliminating block distortions in the restructure image data input from the adding circuit 33 as reference picture data R_PIC.

[0029] [Rate Control Circuit 32]

The rate control circuit 32 generates a quantization scale QS, for example, based on image data read from the buffer memory 28 and outputs the same to the quantization circuit 26.

[0030] [Intra-Prediction Circuit 41]

The intra-prediction circuit 41 determines a mode of intra-prediction and a block size of a prediction block, which give the minimum residual error, in a macro block to be subjected to intra-coding.

The intra-prediction circuit 41 uses 4×4 or 16×16 pixels as a block size.

When intra-prediction is selected, the intra-prediction circuit 41 outputs prediction image data by the intra-prediction to the computing circuit 24.

[0031] [Motion Prediction Compensation Circuit 42]

The motion prediction compensation circuit 42 performs motion prediction on images, which are already encoded, partially decoded and recorded in the frame memory 31, in order and determines a motion vector and a block size of motion compensation, which give the minimum residual error.

The motion prediction compensation circuit 42 uses 16×16, 16×8, 8×16, 8×8, 8×4, 4×8 and 4×4 pixels as a block size.

When inter-prediction is selected, the motion prediction compensation circuit 42 outputs prediction image data by inter-prediction to the computing circuit 24.

[0032] [Orthogonal Transformation Size Determination Circuit 45]

The orthogonal transformation size determination circuit 45 determines an orthogonal transformation size based on a block size finally determined (selected) in either of the intra-prediction circuit 41 or the motion prediction compensation circuit 42, by which the prediction image data is selected, and outputs an orthogonal transformation size signal TRSIZE indicating the above to the orthogonal transformation circuit 25, the quantization circuit 26 and the reversible encoding circuit 27.

Specifically, when a block size of 8×8 pixels is finally selected by the intra-prediction circuit 41, the orthogonal transformation size determination circuit 45 generates an orthogonal transformation size signal TRSIZE indicating 8×8 pixels; while when a block size other than 8×8 is finally selected by the intra-prediction circuit

41, generates an orthogonal transformation size signal TRSIZE indicating 4×4 pixels.

Also, when a block size of 8×8 pixels or larger is finally selected by the motion prediction compensation circuit 42, the orthogonal transformation size determination circuit 45 generates an orthogonal transformation size signal TRSIZE indicating 8×8 pixels; while when a smaller block size than 8×8 pixels is finally selected by the motion prediction compensation circuit 42, generates an orthogonal transformation size signal TRSIZE indicating 4×4 pixels.

In the present embodiment, the orthogonal transformation size determination circuit 45 generates an orthogonal transformation size signal TRSIZE indicating a block size of either of 4×4 or 8×8.

[0033] Below, variable length encoding of the image data S25 in the reversible encoding circuit 27 will be explained in detail.

FIG. 3 is a view of a configuration of the reversible encoding circuit 27 shown in FIG. 2.

As shown in FIG. 3, the reversible encoding circuit 27 has the configuration for performing variable length encoding on the image data S25 and includes, for example, a scanning transformation circuit 51, a sub block generation circuit 52, a run level calculation circuit 53,

a two-dimensional reversible encoding circuit 54, a level encoding circuit 55, a run encoding circuit 56 and a multiplexing circuit 57.

[0034] When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 4×4, the scanning transformation circuit 51 scans 16 of transformation coefficients in 4×4 block data composing the image data S26 in numerical order shown in FIG. 4A in the case of frame encoding and in numerical order shown in FIG. 4B in the case of field encoding, and outputs the same to the sub block generation circuit 52 in the scanned order.

On the other hand, when the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 8×8, the scanning transformation circuit 51 scans 64 of transformation coefficient data in 8×8 block data composing the image data S26 in numerical order shown in FIG. 5 and outputs the same to the sub block generation circuit 52 in the scanned order.

In FIG. 5, the upper left portion indicates direct current DC components and the lower right portion corresponds to high frequency components.

Also, in the FIG. 5, the horizontal direction indicates horizontal frequency components and the

vertical direction indicates vertical frequency components.

[0035] When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 4×4, the sub block generation circuit 52 outputs 16 of transformation coefficients composing the 4×4 block data successively input from the scanning transformation circuit 51 to the run level calculation circuit 53 in order.

Also, when the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 8×8, the sub block generation circuit 52 determines transformation coefficients input first to sixteenth as components of a 4×4 sub block data SB1, transformation coefficients input seventeenth to thirty second as components of a 4×4 sub block data SB2, transformation coefficients input thirty third to fourth eighth as components of a 4×4 sub block data SB3, and transformation coefficients input forty ninth to sixty fourth as components of a 4×4 sub block data SB4 in the 64 transformation coefficients composing the 8×8 block data input from the scanning transformation circuit 51 and outputs these to the run level calculation circuit 53.

[0036] When the orthogonal transformation size

signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 4×4, the run level calculation circuit 53 generates level data "level", run data "run_before", run total quantity data "total_zero", non-0 coefficient quantity data "TotalCoeff", final continuing quantity data "TrailingOnes" and encoding data "trailing_ones_sing_flag" for a series of 16 of transformation coefficients successively input from the sub block generation circuit 52.

[0037] Here, the level data "level" indicates values of respective transformation coefficients (transformation coefficients other than "0" and "1") in the 4×4 block data, which are "-3", "+8", "+11", "-4" and "+23" in the case in FIG. 6.

The run data "run_before" indicates the number of continuing 0 coefficients (transformation coefficients of 0) before a non-0 coefficient in the 4×4 block data, which are "1", "2", "0", "2", "0" and "0" in the case in FIG. 6.

The run total quantity data "total_zero" indicates the number of 0 coefficients before the final non-0 coefficient in the 4×4 block data, which is "5" in the case in FIG. 6.

The non-0 coefficient quantity data "TotalCoeff"

indicates the number of non-0 coefficients in the 4×4 block data, which is "7" in the case in FIG. 6.

The final continuing quantity data "TrailingOnes" indicates the number of continuing transformation coefficients of 1 as an absolute value in the 4×4 block data, which is "2" in the case in FIG. 6.

The encoding data "trailing_ones_sing_flag" indicates codes of continuing transformation coefficients of "1" as an absolute value at the end of the 4×4 block data, which is "-" and "+" in the case in FIG. 6.

[0038] The run level calculation circuit 53 outputs the run data "run_before" and the run total quantity data "total_zero" to the run encoding circuit 56.

The run level calculation circuit 53 outputs the level data "level" to the level encoding circuit 55.

The run level calculation circuit 53 outputs the non-0 coefficient quantity data "TotalCoeff", final continuing quantity data "TrailingOnes" and encoding data "trailing_ones_sing_flag" to the two-dimensional reversible encoding circuit 54.

[0039] When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 4×4, the run level calculation circuit 53 performs the same processing as that in the case of the 4×4 described above

respectively on the 4×4 sub blocks SB1, SB2, SB3 and SB4 input from the sub block generation circuit 52 to generate level data "level", run data "run_before", run total quantity data "total_zero, non-0 coefficient quantity data "TotalCoeff", final continuing quantity data "TrailingOnes" and encoding data "trailing_ones_sing_flag".

[0040] The two-dimensional reversible encoding circuit 54 performs variable length encoding on the non-0 coefficient quantity data "TotalCoeff", final continuing quantity data "TrailingOnes" and encoding data "trailing_ones_sing_flag".

Below, an encoding method of non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" by the two-dimensional reversible encoding circuit 54 will be explained.

First, the case where the orthogonal transformation size signal TRSIZE indicates 4×4 will be explained.

When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 4×4, the two-dimensional reversible encoding circuit 54 generates (retrieves) encoding codes of the non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" of the block data based on the number

of transformation coefficients other than "0" and "1" (or "0") among transformation coefficients in 4×4 block data around the 4×4 block data to be processed and based on total transformation table data TRNa below.

[0041] [Table 1]

The total transformation table data TRNa

TrailingOnes	TotalCoeff	0 <= nC < 2	2 <= nC < 4	4 <= nC < 8	8 <= nC	nC = = -1
		TRNa1	TRNa2	TRNa3	TRNa4	TRNa5
0	0	1	11	1111	0000 11	01
0	1	0001 01	0010 11	0011 11	0000 00	0001 11
1	1	01	10	1110	0000 01	1
0	2	0000 0111	0001 11	0010 11	0001 00	0001 00
1	2	0001 00	0011 1	0111 1	0001 01	0001 10
2	2	001	011	1101	0001 10	001
0	3	0000 0011 1	0000 111	0010 00	0010 00	0000 11
1	3	0000 0110	0010 10	0110 0	0010 01	0000 011
2	3	0000 101	0010 01	0111 0	0010 10	0000 010
3	3	0001 1	0101	1100	0010 11	0001 01
0	4	0000 0001 11	0000 0111	0001 111	0011 00	0000 10
1	4	0000 0011 0	0001 10	0101 0	0011 01	0000 0011
2	4	0000 0101	0001 01	0101 1	0011 10	0000 0010
3	4	0000 11	0100	1011	0011 11	0000 000
0	5	0000 0000 111	0000 0100	0001 011	0100 00	-
1	5	0000 0001 10	0000 110	0100 0	0100 01	-
2	5	0000 0010 1	0000 101	0100 1	0100 10	-
3	5	0000 100	0011 0	1010	0100 11	-
0	6	0000 0000 0111 1	0000 0011 1	0001 001	0101 00	-
1	6	0000 0000 110	0000 0110	0011 10	0101 01	-
2	6	0000 0001 01	0000 0101	0011 01	0101 10	-
3	6	0000 0100	0010 00	1001	0101 11	-
0	7	0000 0000 0101 1	0000 0001 111	0001 000	0110 00	-
1	7	0000 0000 0111 0	0000 0011 0	0010 10	0110 01	-
2	7	0000 0000 101	0000 0010 1	0010 01	0110 10	-
3	7	0000 0010 0	0001 00	1000	0110 11	-
0	8	0000 0000 0100 0	0000 0001 011	0000 1111	0111 00	-
1	8	0000 0000 0101 0	0000 0001 110	0001 110	0111 01	-
2	8	0000 0000 0110 1	0000 0001 101	0001 101	0111 10	-
3	8	0000 0001 00	0000 100	0110 1	0111 11	-
0	9	0000 0000 0011 11	0000 0000 1111	0000 1011	1000 00	-
1	9	0000 0000 0011 10	0000 0001 010	0000 1110	1000 01	-
2	9	0000 0000 0100 1	0000 0001 001	0001 010	1000 10	-
3	9	0000 0000 100	0000 0010 0	0011 00	1000 11	-
0	10	0000 0000 0010 11	0000 0000 1011	0000 0111 1	1001 00	-
1	10	0000 0000 0010 10	0000 0000 1110	0000 1010	1001 01	-
2	10	0000 0000 0011 01	0000 0000 1101	0000 1101	1001 10	-
3	10	0000 0000 0110 0	0000 0001 100	0001 100	1001 11	-
0	11	0000 0000 0001 111	0000 0000 1000	0000 0101 1	1010 00	-
1	11	0000 0000 0001 110	0000 0000 1010	0000 0111 0	1010 01	-
2	11	0000 0000 0010 01	0000 0000 1001	0000 1001	1010 10	-
3	11	0000 0000 0011 00	0000 0001 000	0000 1100	1010 11	-
1	12	0000 0000 0001 010	0000 0000 0111 0	0000 0101 0	1011 01	-
2	12	0000 0000 0001 101	0000 0000 0110 1	0000 0110 1	1011 10	-
3	12	0000 0000 0010 00	0000 0000 1100	0000 1000	1011 11	-
0	13	0000 0000 0000 1111	0000 0000 0101 1	0000 0011 01	1100 00	-
1	13	0000 0000 0000 001	0000 0000 0101 0	0000 0011 1	1100 01	-
2	13	0000 0000 0001 001	0000 0000 0100 1	0000 0100 1	1100 10	-
3	13	0000 0000 0001 100	0000 0000 0110 0	0000 0110 0	1100 11	-
0	14	0000 0000 0000 1011	0000 0000 0011 1	0000 0010 01	1101 00	-
1	14	0000 0000 0000 1110	0000 0000 0010 11	0000 0011 00	1101 01	-
2	14	0000 0000 0000 1101	0000 0000 0011 0	0000 0010 11	1101 10	-
3	14	0000 0000 0001 000	0000 0000 0100 0	0000 0010 10	1101 11	-
0	15	0000 0000 0000 0111	0000 0000 0010 01	0000 0001 01	1110 00	-
1	15	0000 0000 0000 1010	0000 0000 0010 00	0000 0010 00	1110 01	-
2	15	0000 0000 0000 1001	0000 0000 0010 10	0000 0001 11	1110 10	-
3	15	0000 0000 0000 1100	0000 0000 0000 1	0000 0001 10	1110 11	-
0	16	0000 0000 0000 0100	0000 0000 0001 11	0000 0000 01	1111 00	-
1	16	0000 0000 0000 0110	0000 0000 0001 10	0000 0001 00	1111 01	-
2	16	0000 0000 0000 0101	0000 0000 0001 01	0000 0000 11	1111 10	-
3	16	0000 0000 0000 1000	0000 0000 0001 00	0000 0000 10	1111 11	-

[0042] The total transformation table data TRNa in Table 1 above regulates five transformation table data TRNa1, 2, 3, 4 and 5.

The transformation table data TRNa1, 2, 3 and 4 have the following characteristics.

Each of the transformation table data TRNa1, 2, 3 and 4 regulates an encoding code of a set of non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes".

Here, the transformation table data TRNa1, 2, 3 and 4 are regulated, so that the bit lengths of the non-0 coefficient quantity data "TotalCoeff" indicating "0" are different from one another and the maximum bit length of the encoding code becomes longer as the bit length of the non-0 coefficient quantity data "TotalCoeff" indicating "0" becomes shorter.

When the 4×4 block data positions at a complicated image region, there is little possibility that the non-0 coefficient quantity data "TotalCoeff" becomes "0", and there is a characteristic that the values are dispersed in a wide range from 0 to 15.

Also, when the 4×4 block data positions at a flat image region with a little changes, there is high possibility that the non-0 coefficient quantity data "TotalCoeff" becomes "0", and there is a characteristic

that the value scarcely becomes high.

Accordingly, by regulating the transformation table data TRNa1, 2, 3 and 4 as above, transformation table data, wherein a bit length of an encoding code to be assigned to non-0 coefficient quantity data "TotalCoeff" indicating "0" is long but the maximum bit length in the encoding code is short, is selected for a 4×4 block data in a complicated image region, so that the entire encoding efficiency is improved.

On the other hand, transformation table data, wherein the maximum bit length in the encoding code is long but an encoding code to be assigned to non-0 coefficient quantity data "TotalCoeff" indicating "0" is short, is selected for a 4×4 block data in a flat image region, so that the entire encoding efficiency is improved.

[0043] Also, for a plurality of sets, wherein final continuing quantity data "TrailingOnes" is different but non-0 coefficient quantity data "TotalCoeff" is same, it is regulated, so that a bit length of an encoding code becomes the same or longer as the final continuing quantity data "TrailingOnes" becomes larger.

[0044] As shown in FIG. 7A and FIG. 7B, the two-dimensional reversible encoding circuit 54 determines the number of transformation coefficients other than "0" and

"1" (or "0") in adjacent 4×4 block data A to be displayed on the left of the 4×4 block data C to be processed as "nA", and the number of transformation coefficients other than "0" and "1" (or "0") in adjacent 4×4 block data A to be displayed above the 4×4 block data C to be processed as "nB".

Then, the two-dimensional reversible encoding circuit 54 generates index data "nC" from "nC = (nA+nB+1) >> 1".

Wherein ">>1" indicates shifting by "1" to the right.

The two-dimensional reversible encoding circuit 54 selects one of transformation table data TRNa1, 2, 3, 4 and 5 regulated by the total transformation table data TRNa shown in Table 1 based on the index data "nC".

When nA=2 and nB=3, nC = (2+3+1) >> 1 = 3 stands, and the two-dimensional reversible encoding circuit 54 selects the transformation table data TRNa2.

The two-dimensional reversible encoding circuit 54 uses the transformation table data TRNa5 for encoding a DC value of a color difference signal.

Then, the two-dimensional reversible encoding circuit 54 retrieves encoding codes of non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" in the above 4×4 block data by using

the selected transformation table data TRNa1, 2, 3, 4 and 5, and outputs the same to the multiplexing circuit 57.

[0045] Next, the case where the orthogonal transformation size signal TRSIZE indicates 8×8 will be explained.

The four sub block data SB1, SB2, SB3 and SB4 generated by the sub block generation circuit 52 can be expressed as shown in FIG. 8.

In FIG. 8, the upper left portion of the rectangular shape indicates low frequency components and the lower right portion indicates high frequency components.

Accordingly, there is a relatively high possibility that non-0 coefficients exist in the sub block data SB1, while there is high probability that almost all coefficients becomes "0" in the sub block data SB4.

Therefore, for attaining high encoding efficiency, an encoding code having a short encoding length should be assigned to a value "0" (a small value) in the sub block data SB4 and, inversely, an encoding code having a short encoding length should be assigned to a large value in the sub block data SB1.

Here, when the orthogonal transformation size signal TRSIZE indicates 8×8, index data "nC" is generated based on any one of (method 1) to (method 4) described

below.

Note that, the method for generating the index data "nC" is the same in the decoding apparatus 3.

[0046] (Method 1)

When assuming that the 8×8 block data C shown in FIG. 9 is to be processed, the two-dimensional reversible encoding circuit 54 determines that index data "nC" of the sub block SB1 is "8", index data "nC" of the sub block SB2 and SB3 is "4" and index data "nC" of the sub block SB4 is "0".

Therefore, the two-dimensional reversible encoding circuit 54 uses transformation table data TRNa4 shown in Table 1 for encoding the sub block SB1, uses transformation table data TRNa3 for encoding the sub blocks SB2 and SB3, and uses transformation table data TRNa1 for encoding the sub block SB4.

[0047] (Method 2)

When assuming that the 8×8 block data C shown in FIG. 9 is to be processed, the two-dimensional reversible encoding circuit 54 determines that index data "nC" of the sub block SB1 is "8", index data "nC" of the sub block SB2 and SB3 is "2" and index data "nC" of the sub block SB4 is "0".

Therefore, the two-dimensional reversible encoding circuit 54 uses transformation table data TRNa4 shown in

Table 1 for encoding the sub block SB1, uses transformation table data TRNa2 for encoding the sub blocks SB2 and SB3, and uses transformation table data TRNa1 for encoding the sub block SB4.

[0048] (Method 3)

When assuming that the 8×8 block data C shown in FIG. 9 is to be processed, the two-dimensional reversible encoding circuit 54 determines that index data "nC" of the sub block SB1 is "4", index data "nC" of the sub block SB2 and SB3 is "2" and index data "nC" of the sub block SB4 is "0".

Therefore, the two-dimensional reversible encoding circuit 54 uses transformation table data TRNa3 shown in Table 1 for encoding the sub block SB1, uses transformation table data TRNa2 for encoding the sub blocks SB2 and SB3, and uses transformation table data TRNa1 for encoding the sub block SB4.

[0049] (Method 4)

When adjacent block data A and B on the left and above the block data C to be processed as shown in FIG. 9 are orthogonally transformed by 8×8, the two-dimensional reversible encoding circuit 54 generates index data "nC" of the sub block data SB1, SB2, SB3 and SB4 in the block data C by using "nA" and "nB" of sub block data SB1, SB2, SB3 and SB4 at the same positions in the block data A and

B.

For example, the two-dimensional reversible encoding circuit 54 uses "nA" of the sub block data SB1 in the block data A and "nB" of the sub block data SB1 in the block data B to generate index data "nC" of the sub block data SB1 in the block data C from "nC = (nA+nB+1) >> 1".

Also, when one of the block data A and B is orthogonally transformed by 8×8 and the other is orthogonally transformed by 4×4, the two-dimensional reversible encoding circuit 54 determines the number of coefficients other than "0" and "1" (or "0") in sub block data SB1, SB2, SB3 and SB4 at the same positions in the 8×8 orthogonal transformation as index data "nC".

For example, when the block data A is 8×8 and the block data B is 4×4, the two-dimensional reversible encoding circuit 54 determines the number "nA" of coefficients other than "0" and "1" (or "0") in the block data A as index data "nC" of the sub block data SB1 in the block data C.

Also, when both of the block data A and B are 4×4, the two-dimensional reversible encoding circuit 54 uses "nA" and "nB" of sub block data SB1, SB2, SB3 and SB4 in the block data A and B at the same positions of the sub block data SB1, SB2, SB3 and SB4 in the block data C to

generate index data "nC" of the sub block data SB1, SB2, SB3 and SB4 in the block data C from "nC = (nA+nB+1) >> 1".

Note that the above methods of generating index data "nC" are just examples and the method is not particularly limited as far as it uses "nA" and "nB" of sub block data SB1, SB2, SB3 and SB4 to generate index data "nC" of the sub block data SB1, SB2, SB3 and SB4 in the block data C.

The two-dimensional reversible encoding circuit 54 transforms the sub block data SB1, SB2, SB3 and SB4 in the block data C by using transformation table data TRNa1 to 5 selected based on the index data "nC" corresponding thereto.

[0050] Note that, when both of the block data A and B are 4×4 in the method 4, the two-dimensional reversible encoding circuit 54 may determine index data "nC" of the sub block data SB1, SB2, SB3 and SB4 in the block data C in accordance with positions of sub block data SB1, SB2, SB3 and SB4 thereof as in any one of the (method 1), (method 2) and (method 3).

[0051] As explained above, when the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 8×8, the two-dimensional reversible encoding

circuit 54 determines or generates index data "nC" for four sub block data SB1, SB2, SB3 and SB4 generated by the sub block generation circuit 52 from the 8×8 block data to be processed.

Then, the two-dimensional reversible encoding circuit 54 selects one of the transformation table data TRNa1 to 5 shown in Table 1 based on the above determined or generated index data "nC".

The two-dimensional reversible encoding circuit 54 uses the selected transformation table data TRNa1 to 5 to retrieve encoding codes of non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" of the block data to be processed.

[0052] Below, an operation example of determining encoding codes of non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" obtained from each block data in the image data S26 in the reversible encoding circuit 27 shown in FIG. 3 will be explained.

FIG. 10 is a flowchart for explaining the operation example.

Below, each step in FIG. 10 will be explained.

Step ST11:

When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size

determination circuit 45 shown in FIG. 2 indicates 4×4, the reversible encoding circuit 27 shown in FIG. 3 proceeds to a step ST17 and, then, processing in steps ST17 to ST22 is performed.

On the other hand, when the orthogonal transformation size signal TRSIZE indicates 4×4, the reversible encoding circuit 27 proceeds to a step ST12 and, then, processing in steps ST12 to ST16 is performed.

[0053] Step ST12:

When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 4×4, the scanning transformation circuit 51 scans 16 of transformation coefficients in 4×4 block size composing the image data S26 in numerical order shown in FIG. 4A at the time of frame encoding or in numerical order shown in FIG. 4B at the time of field encoding, and outputs the same to the sub block generation circuit 52 in the scanned order.

The sub block generation circuit 52 outputs the transformation coefficients input from the scanning transformation circuit 51 as they are to the run level calculation circuit 53.

Step ST13:

When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size

determination circuit 45 indicates 4×4, the run level calculation circuit 53 generates level data "level", run data "run_before", run total quantity data "total_zero, non-0 coefficient quantity data "TotalCoeff", final continuing quantity data "TrailingOnes" and encoding data "trailing_ones_sing_flag" for a series of the 16 transformation coefficients input successively from the sub block generation circuit 52.

The run level calculation circuit 53 outputs non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" to the two-dimensional reversible encoding circuit 54.

[0054] Step ST14:

The two-dimensional reversible encoding circuit 54 determines, as shown in FIG. 7A and FIG. 7B, the number of transformation coefficients other than "0" and "1" (or "0") in adjacent 4×4 block data A to be displayed on the left of 4×4 block data C to be processed is "nA", and the number of transformation coefficients other than "0" and "1" (or "0") in adjacent 4×4 block data B to be displayed above the 4×4 block data C to be processed is "nB".

Then, the two-dimensional reversible encoding circuit 54 generates index data "nC" from "nC = (nA+nB+1) >> 1".

Step ST15:

The two-dimensional reversible encoding circuit 54 selects one of transformation table data TRNa1 to 5 shown in Table 1 based on the index data "nC" generated at the step ST14.

Step ST16:

The two-dimensional reversible encoding circuit 54 retrieves encoding codes of non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" of the 4×4 block data input at the step ST13 by using the transformation table data TRANa1, 2, 3, 4 and 5 selected at the step ST15 and outputs the same to the multiplexing circuit 57.

[0055] Step ST17:

When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 8×8, the scanning transformation circuit 51 scans 64 of transformation coefficient data in the 8×8 block data composing the image data S26 in numerical order shown in FIG. 5 and outputs the same to the sub block generation circuit 52 in the scanned order.

[0056] Step ST18:

When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 4×4, the sub block

generation circuit 52 outputs 16 of transformation coefficients composing the 4×4 block data input successively from the scanning transformation circuit 51 to the run level calculation circuit 53 in order.

When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 8×8, the sub block generation circuit 52 determines transformation coefficients input first to sixteenth as components of a 4×4 sub block data SB1, transformation coefficients input seventeenth to thirty second as components of a 4×4 sub block data SB2, transformation coefficients input thirty third to fourth eighth as components of a 4×4 sub block data SB3, and transformation coefficients input forty ninth to sixty fourth as components of a 4×4 sub block data SB4 in the 64 of transformation coefficients composing the 8×8 block data input from the scanning transformation circuit 51 and outputs these to the rub level calculation circuit 53.

[0057] Step ST19:

When the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 indicates 8×8, the run level calculation circuit 53 performs the same processing as that in the case of 4×4 explained above to generate level

data "level", run data "run_before", run total quantity data "total_zero, non-0 coefficient quantity data "TotalCoeff", final continuing quantity data "TrailingOnes" and encoding data "trailing_ones_sing_flag" for the respective 4×4 sub block data SB1, SB2, SB3 and SB4 input from the sub block generation circuit 52.

The run level calculation circuit 53 outputs non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" to the two-dimensional reversible encoding circuit 54.

[0058] Step ST20:

The two-dimensional reversible encoding circuit 54 determines or generates index data "nC" for the respective sub block data SB1, SB2, SB3 and SB4 composing the 8×8 block data to be processed by following any one of the (method 1) to (method 5) described above.

Step ST21:

The two-dimensional reversible encoding circuit 54 selects one of the transformation table data TRNa1 to 5 shown in Table 1 based on the index data "nC" determined or generated at the step ST20.

Step ST22:

The two-dimensional reversible encoding circuit 54 retrieves encoding codes of non-0 coefficient quantity

data "TotalCoeff" and final continuing quantity data "TrailingOnes" of the respective sub block data SB1, SB2, SB3 and SB4 input at the step ST19 by using the transformation table data TRNa1, 2, 3, 4 and 5 selected at the step ST21 and outputs the same to the multiplexing circuit 57.

[0059] Below, the level encoding circuit 55 will be explained.

The level encoding circuit 55 performs variable length encoding on the level data "level" input from the run level calculation circuit 53.

Specifically, the level encoding circuit 55 extracts parameters called "level_prefix" and "level_suffix" from the level data "level".

Then, the level encoding circuit 55 performs variable length encoding on the parameter "level_prefix" based on the transformation table data TRNb shown in Table 2 below.

[0060] [Table 2]

The transformation table data TRNb

level_prefix	Bit String
0	1
1	01
2	001
3	0001
4	0000 1
5	0000 01
6	0000 001
7	0000 0001
8	0000 0000 1
9	0000 0000 01
10	0000 0000 001
11	0000 0000 0001
12	0000 0000 0000 1
13	0000 0000 0000 01
14	0000 0000 0000 001
15	0000 0000 0000 0001

[0061] The parameter "level_suffix" is encoded as an unsigned integer by a bit length given by "suffxLength".

Here, a relationship of the level data "level" and the parameters "level_prefix" and "level_suffix" is regulated by the following formulas (1) and (2).

[0062] [Formula 1]

levelCode = (level_prefix << suffxLength) + level_suffix ...(1)

[0063] [Formula 2]

when "levelCode" is even number: level = (levelCode + 2) >> 1

when "levelCode" is not even number: level = (-levelCode - 1) >> 1

...(2)

[0064] The level encoding circuit 55 outputs

encoding code obtained by performing variable length encoding on the level data "level" to the multiplexing circuit 57.

[0065] Below, the run encoding circuit 56 will be explained.

The run encoding circuit 56 performs variable length encoding on the run data "run_before" and run total quantity data "total_zero" input from the run level calculation circuit 53 as described below.

Then, the run encoding circuit 56 outputs encoding code obtained by performing the variable length encoding to the multiplexing circuit 57.

Specifically, when the orthogonal transformation size signal TRSIZE indicates 4×4 and the non-0 coefficient quantity data "TotalCoeff" is 1 or larger and 7 or smaller, the run encoding circuit 56 performs variable length encoding on the run total quantity data "total_zero" based on the transformation table data TRNc shown in Table 3 below.

[0066] [Table 3]

The transformation table data TRNc

total_zeros	TotalCoeff						
	1	2	3	4	5	6	7
0	1	111	0101	0001 1	0101	0000 01	0000 01
1	011	110	111	111	0100	0000 1	0000 1
2	010	101	110	0101	0011	111	101
3	0011	100	101	0100	111	110	100
4	0010	011	0100	110	110	101	011
5	0001 1	0101	0011	101	101	100	11
6	0001 0	0100	100	100	100	011	010
7	0000 11	0011	011	0011	011	010	0001
8	0000 10	0010	0010	011	0010	0001	001
9	0000 011	0001 1	0001 1	0010	0000 1	001	0000 00
10	0000 010	0001 0	0001 0	0001 0	0001	0000 00	
11	0000 0011	0000 11	0000 01	0000 1	0000 0		
12	0000 0010	0000 10	0000 1	0000 0			
13	0000 0001 1	0000 01	0000 00				
14	0000 0001 0	0000 00					
15	0000 0000 1						

[0067] Also, when the orthogonal transformation size signal TRSIZE indicates 4×4 and the non-0 coefficient quantity data "TotalCoeff" is 8 or larger and 15 or smaller, the run encoding circuit 56 performs variable length encoding on the run total quantity data "total_zero" based on the transformation table data TRNd shown in Table 4 below.

[0068] [Table 4]

The transformation table data TRNd

total_zeros	TotalCoeff							
	8	9	10	11	12	13	14	15
0	0000 01	0000 01	0000 1	0000	0000	000	00	0
1	0001	0000 00	0000 0	0001	0001	001	01	1
2	0000 1	0001	001	001	01	1	1	
3	011	11	11	010	1	01		
4	11	10	10	1	001			
5	10	001	01	011				
6	010	01	0001					
7	001	0000 1						
8	0000 00							

[0069] Also, when the block data to be encoded is color difference DC of 2×2, the run encoding circuit 56 performs variable length encoding on the run total quantity data "total_zero" based on the transformation table data TRNe shown in Table 5 below.

[0070] [Table 5]

The transformation table data TRNe

total_zeros	TotalCoeff		
	1	2	3
0	1	1	1
1	01	01	0
2	001	00	
3	000		

[0071] Also, the run encoding circuit 56 performs variable length encoding on the run data "run_before" based on the transformation table data TRNf shown in Table 6 below.

[0072] [Table 6]

The transformation table data TRNf

run_before	zerosLeft						
	1	2	3	4	5	6	>6
0	1	1	11	11	11	11	111
1	0	01	10	10	10	000	110
2	-	00	01	01	011	001	101
3	-	-	00	001	010	011	100
4	-	-	-	000	001	010	011
5	-	-	-	-	000	101	010
6	-	-	-	-	-	100	001
7	-	-	-	-	-	-	0001
8		-	-	-	-	-	00001
9	-	-	-	-	-	-	000001
10	-	-	-	-	-	-	0000001
11	-	-	-	-	-	-	00000001
12	-	-	-	-	-	-	000000001
13	-	-	-	-	-	-	0000000001
14	-	-	-	-	-	-	00000000001

[0073] The run encoding circuit 56 outputs encoding codes obtained by performing variable length encoding on run total quantity data "total_zero and the run data "run_before" to the multiplexing circuit 57.

[0074] The multiplexing circuit 57 generates image data S27 as a bit stream obtained by multiplexing the encoding codes input from the two-dimensional reversible encoding circuit 54, the level encoding circuit 55 and

the run encoding circuit 56 and writes the same in the buffer memory 28.

[0075] Below, an overall operation of the encoding apparatus 2 shown in FIG. 2 will be explained.

An image signal as an input is converted to a digital signal in the A/D conversion circuit 22 first.

Next, relocating of frame image data is performed in the screen relocating circuit 23 in accordance with the GOP structure of image compression information to be output, and original image data S23 obtained thereby is output to the computing circuit 24, the motion prediction compensation circuit 42 and the intra-prediction circuit 41.

Next, the computing circuit 24 detects a difference between the original image data S23 from the screen relocating circuit 23 and prediction image data PI from the selection circuit 44 and outputs image data S24 indicating the difference to the orthogonal transformation circuit 25.

[0076] Next, the orthogonal transformation circuit 25 performs orthogonal transformation, such as discrete cosine transformation and Karhunen-Loeve transformation, on the image data S24 based on a block size indicated by the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination

circuit 45 to generate image data (DCT coefficient) S25 and outputs the same to the quantization circuit 26.

Next, the quantization circuit 26 performs quantization on the image data S25 based on a block size indicated by the orthogonal transformation size signal TRSIZE input from the orthogonal transformation size determination circuit 45 and outputs image data (quantized DCT coefficient) S26 to the reversible encoding circuit 27 and the inverse quantization circuit 29.

Next, as described above, the reversible encoding circuit 27 performs variable length encoding on the image data S26 to generate image data S27 and accumulates the same in the buffer memory 28.

Also, the rate control circuit 32 controls a quantization rate in the quantization circuit 26 based on the image data read from the buffer memory 28.

[0077] Also, the inverse quantization circuit 29 performs inverse quantization on the image data S26 input from the quantization circuit 26 and outputs the result to the inverse orthogonal transformation circuit 30.

Then, the inverse orthogonal transformation circuit 30 outputs image data generated by performing inverse transformation processing of that in the orthogonal transformation circuit 25 to the adding circuit 33.

In the adding circuit 33, the image data from the inverse orthogonal transformation circuit 30 and the prediction image data PI from the selection circuit 44 are added to generate reference image data "R_PIC", which is written in the frame memory 31.

[0078] Also, the intra-prediction circuit 41 performs intra-prediction encoding by block sizes of 4×4 and 16×16 on the block data read from the frame memory 31 and generates the prediction image data.

Also, the motion prediction compensation circuit 42 performs inter-prediction encoding by block sizes of 16×16, 16×8, 8×16, 8×8, 8×4 and 4×8 on the block data read from the frame memory 31 and generates the prediction image data.

Then, among the prediction image data of the intra-prediction circuit 41 and the motion prediction compensation circuit 42, prediction image data with the minimum encoding cost is output to the computing circuit 24.

[0079] The orthogonal transformation size determination circuit 45 outputs an orthogonal transformation size signal TRSIZE indicating a block size used for generating the prediction image data output to the computing circuit 24 to the orthogonal transformation circuit 25, the quantization circuit 26 and the

reversible encoding circuit 27.

[0080] As explained above, according to the encoding apparatus 2, in the reversible encoding circuit 27 shown in FIG. 3, by using the total transformation table data TRANa shown in Table 1 used for encoding transformation coefficients subjected to orthogonal transformation by 4×4, non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" of transformation coefficients subjected to orthogonal transformation by 8×8 can be encoded.

Also, according to the encoding apparatus 2, in the reversible encoding circuit 27, transformation table data TRNa, a2, a3 and a4 used for encoding sub block data SB1, SB2, SB3 and SB4 are selected by the (method 1) to (method 4), so that highly efficient encoding can be realized.

[0081] [Decoding Apparatus 3]

Below, the decoding apparatus 3 shown in FIG. 1 will be explained.

FIG. 11 is a view of a configuration of the decoding apparatus 3 shown in FIG. 1.

As shown in FIG. 11, the decoding apparatus 3 includes, for example, a buffer memory 81, a reversible decoding circuit 82, an inverse quantization circuit 83, an inverse orthogonal transformation circuit 84, an

adding circuit 85, a frame memory 86, a screen relocating buffer 87, a D/A conversion circuit 88, an intra-prediction circuit 89 and a motion prediction compensation circuit 90.

[0082] The buffer memory 81 stores image data S2 as a bit stream received (input) from the encoding apparatus 2.

The inverse decoding circuit 82 decodes the image data S2 read from the buffer memory 81 by a method corresponding to inverse encoding by the inverse encoding circuit 27 shown in FIG. 2 and generates image data S82.

The inverse decoding circuit 82 separates and decodes the orthogonal transformation size signal TRSIZE multiplexed to be image data S2 and outputs the result to the inverse quantization circuit 83 and the inverse orthogonal transformation circuit 84.

The inverse decoding circuit 82 will be explained in detail later on.

[0083] The inverse quantization circuit 83 generates image data S83 by performing inverse quantization by an inverse quantization method corresponding to the quantization method by the quantization circuit 26 shown in FIG. 2 on the image data S82 subjected to reversible decoding input from the reversible decoding circuit 82 based on the orthogonal transformation size signal TRSIZE

input from the reversible decoding circuit 82 and outputs the same to the inverse orthogonal transformation circuit 84.

The inverse orthogonal transformation circuit 84 generates image data S84 by performing inverse orthogonal transformation corresponding to the orthogonal transformation by the orthogonal transformation circuit 25 shown in FIG. 2 on the image data S83 input from the inverse quantization circuit 83 based on the orthogonal transformation size signal TRSIZE input from the reversible decoding circuit 82 and outputs the same to the adding circuit 85.

The adding circuit 85 generates image data S85 by adding the prediction image input from the intra-prediction circuit 89 or the motion prediction compensation circuit 90 and the image data S84 input from the inverse orthogonal transformation circuit 84 and outputs the same to the frame memory 86 and the screen relocating buffer 87.

The screen relocating buffer 87 is used for relocating the image data S85 input from the adding circuit 85 to be in an order of being displayed in units of picture and reading out the same to the D/A conversion circuit 88.

The D/A conversion circuit 88 performs D/A

conversion on the image data read from the screen relocating buffer 87 and generates an analog image signal.

[0084] When the block data to be processed in the image data S85 read from the frame memory 86 is subjected to intra-prediction encoding, the intra-prediction circuit 89 decodes the block data by an intra method to generate prediction image data and outputs the same to the adding circuit 85.

When the block data to be processed in the image data S85 read from the frame memory 86 is subjected to inter-prediction encoding, the motion prediction compensation circuit 90 decodes the block data by an inter method to generate prediction image data and outputs the same to the adding circuit 85.

[0085] Below, the reversible decoding circuit 82 shown in FIG. 11 will be explained.

FIG. 12 is a view of a configuration of the reversible decoding circuit 82 shown in FIG. 11.

As shown in FIG. 12, the reversible decoding circuit 82 includes, for example, a separation circuit 110, a two-dimensional reversible decoding circuit 111, a level decoding circuit 112, a run decoding circuit 113, a transformation coefficient recovery circuit 114, a block recovery circuit 115 and a scanning conversion circuit 116.

In the present embodiment, processing in the two-dimensional reversible decoding circuit 111, the level decoding circuit 112, the run decoding circuit 113, the transformation coefficient recovery circuit 114, the block recovery circuit 115 and the scanning conversion circuit 116 is performed by using an orthogonal transformation size signal TRSIZE separated by the separation circuit 110.

[0086] The separation circuit 110 separates (extracts) encoding codes of run data "run_before" and run total quantity data "total_zero" from the encoded image data S2 and outputs the same to the run decoding circuit 113.

Also, the separation circuit 110 separates an encoding code of level data "level" from the image data S2 and outputs the same to the level decoding circuit 112.

The separation circuit 110 separates encoding codes of non-0 coefficient quantity data "TotalCoeff", final continuing quantity data "TrailingOnes" and encoding data "trailing_ones_sing_flag" from the image data S2 and outputs the same to the two-dimensional reversible decoding circuit 111.

Also, the separation circuit 110 separates the orthogonal transformation size signal TRSIZE from the image data S2 and outputs the same to the two-dimensional

reversible decoding circuit 111, the level decoding circuit 112, the run decoding circuit 113, the transformation coefficient recovery circuit 114, the block recovery circuit 115 and the scanning conversion circuit 116 shown in FIG. 12 and the inverse quantization circuit 83 and the inverse orthogonal transformation circuit 84 shown in FIG. 11.

[0087] The two-dimensional reversible decoding circuit 111 selects one of the transformation table data TRNa1 to 5 in the total transformation table data shown in Table 1 described above by using the orthogonal transformation size signal TRSIZE by the same method as that in the two-dimensional reversible decoding circuit 54 shown in FIG. 3 described above.

Then, the two-dimensional reversible decoding circuit 111 decodes the encoding codes input from the separation circuit 110 by using the selected transformation table data TRNa1 to 5, retrieves non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" and outputs the same to the transformation coefficient recovery circuit 114.

Also, the two-dimensional reversible decoding circuit 111 decodes the encoding codes separated by the separation circuit 110, retrieves encoding data

"trailing_ones_sing_flag" and outputs the same to the transformation coefficient recovery circuit 114.

[0088] The level decoding circuit 112 performs decoding corresponding to the variable length encoding by the level encoding circuit 55 shown in FIG. 3 by using the transformation table data TRNb shown in Table 2 described above, retrieves level data "level" corresponding to the encoding code input from the separation circuit 110 and outputs the same to the transformation coefficient recovery circuit 114.

[0089] The run decoding circuit 113 performs decoding corresponding to variable length coding by the run encoding circuit 56 shown in FIG. 3 by using the transformation table data TRNc, TRNd, TRNe and TRNf shown in Table 3, Table 4, Table 5 and Table 6 described above, retrieves run data "run_before" and run total quantity data "total_zero" corresponding to the encoding codes from the separation circuit 110, and outputs the same to the transformation coefficient recovery circuit 114.

[0090] The transformation coefficient recovery circuit 114 generates transformation coefficients by performing inverse processing of the processing by the run level calculation circuit 53 shown in FIG. 3 based on the non-0 coefficient quantity data "TotalCoeff", final continuing quantity data "TrailingOnes" and encoding data

"trailing_ones_sing_flag" input from the two-dimensional reversible decoding circuit 111 and run data "run_before" and run total quantity data "total_zero" input from the run decoding circuit 113 and outputs the same to the block recovery circuit 115.

[0091] When the orthogonal transformation size signal TRSIZE indicates 4×4, the block recovery circuit 115 stores transformation coefficients for the 4×4 input from the transformation coefficient recovery circuit 114.

When the orthogonal transformation size signal TRSIZE indicates 8×8, the block recovery circuit 115 stores transformation coefficients for the 8×8 input from the transformation coefficient recovery circuit 114.

[0092] When the orthogonal transformation size signal TRSIZE indicates 4×4, the scanning transformation circuit 116 reads transformation coefficients for the 4×4 stored in the transformation coefficient recovery circuit 114 in an order suitable to inverse quantization by the inverse quantization circuit 83 shown in FIG. 11 and outputs the same as image data S82 to the inverse quantization circuit 83.

Also, when the orthogonal transformation size signal TRSIZE indicates 8×8, the scanning transformation circuit 116 reads transformation coefficients for the 8×8 stored in the transformation coefficient recovery circuit

114 in the scanning order shown in FIG. 5 and in an order suitable to inverse quantization by the inverse quantization circuit 83 shown in FIG. 11 in consideration of an arrangement of the sub block data SB1, SB2, SB3 and SB4 shown in FIG. 8 and outputs the same as image data S82 to the inverse quantization circuit 83.

[0093] According to the decoding apparatus 3, encoding codes of the non-0 coefficient quantity data "TotalCoeff" and final continuing quantity data "TrailingOnes" encoded by the encoding apparatus 2 can be recovered.

[0094] The present invention is not limited to the above embodiments.

For example, in the above embodiments, the total transformation table data TRNa shown in Table 1 was mentioned as an example of correspondence data for encoding the non-0 coefficient quantity data "TotalCoeff", final continuing quantity data "TrailingOnes", however, other transformation table data may be used as the transformation table data TRNa1, 2, 3 and 4 as far as it is regulated, so that bit lengths of the non-0 coefficient quantity data "TotalCoeff" indicating "0" are different from one another and the maximum bit length of the encoding code becomes longer as the bit length of the non-0 coefficient quantity data "Total Coeff" indicating

"0" becomes shorter.

[0095] Also, in the encoding apparatus 2 described above, the case of realizing the encoding processing shown in FIG. 10 by circuits composing the reversible encoding circuit 27 shown in FIG. 3 was explained as an example, but all or a part of the processing may be performed by a CPU (central processing unit), etc. in accordance with description in the program.

Also, in the decoding apparatus 3 explained above, the case of realizing the decoding processing by circuits composing the reversible decoding circuit 82 shown in FIG. 11 was explained as an example, but all or a part of the processing may be performed by a CPU, etc. in accordance with description in the program.

INDUSTRIAL APPLICABILITY

[0096] The present invention can be applied to an encoding system, etc. for encoding transformation coefficients of orthogonal transformation.